Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 14. (canceled)

15. (previously presented) A composite switch comprising:

a first integrated circuit for outputting a first time-division multiplexed signal that comprises a first series of frame boundaries to a second integrated circuit and for outputting a second time-division multiplexed signal that comprises a second series of frame boundaries to a third integrated circuit;

wherein said second integrated circuit comprises:

(i) a first input port for receiving said first time-division multiplexed signal,

(ii) a first memory that stores said first time-division multiplexed signal at a location that is indicated by a first write pointer and that reads said first time-division multiplexed signal at a location that is indicated by a first read pointer,

(iii) a first frame position register whose contents are related to how far said first time-division multiplexed signal is from a frame boundary in said first time-division multiplexed signal at a first point in time, and

(iv) a first output port for outputting a third time-division multiplexed signal that is based on said first time-division multiplexed signal and that comprises a third series of frame boundaries;

wherein said third integrated circuit comprises:

(i) a second input port for receiving said second time-division multiplexed signal,

(ii) a second memory that stores said second time-division multiplexed signal at a location that is indicated by a second write pointer and that

reads said second time-division multiplexed signal at a location that is indicated by a second read pointer,

(iii) a second frame position register whose contents are related to how far said second time-division multiplexed signal is from a frame boundary in said second time-division multiplexed signal at said first point in time, and

(iv) a second output port for outputting a fourth time-division multiplexed signal that is based on said second time-division multiplexed signal and that comprises a fourth series of frame boundaries;

a fourth integrated circuit comprising:

(i) a third input port for receiving said third time-division multiplexed signal,

(ii) a third memory that stores said third time-division multiplexed signal at a location that is indicated by a third write pointer and that reads said second time-division multiplexed signal at a location that is indicated by a third read pointer,

(iii) a third frame position register whose contents are related to how far said third time-division multiplexed signal is from a frame boundary in said third time-division multiplexed signal at a second point in time,

(iv) a fourth input port for receiving said fourth time-division multiplexed signal,

(v) a fourth memory that stores said fourth time-division multiplexed signal at a location that is indicated by a fourth write pointer and that reads said fourth time-division multiplexed signal at a location that is indicated by a fourth read pointer,

(vi) a fourth frame position register whose contents are related to how far said fourth time-division multiplexed signal is from a frame boundary in said fourth time-division multiplexed signal at said second point in time; and

a controller for reading the contents of said first frame position register and said second frame position register, for storing a value in said first read pointer based on the

contents of said first frame position register and said second frame position register, for reading the contents of said third frame position register and said fourth frame position register, and for storing a value in said third read pointer based on the contents of said third frame position register and said fourth frame position register.

16. (previously presented) The composite switch of claim 15 wherein said first point in time and said second point in time are the same.

17. – 27 (canceled)

28. (previously presented) A method comprising:

transmitting a frame synchronization signal to frame position registers of multiple SONET/SDH switches;

reading contents of the frame position registers in response to the frame synchronization signal;

normalizing the contents of the frame position registers;

determining the largest propagation delay from the normalized contents of the frame position registers;

determining port-specific offsets for read pointer offset registers of the multiple SONET/SDH switches as a function of the longest propagation delay; and

writing the port-specific offsets into the read pointer offset registers.